Fabrication of MOS-Capacitors for characterization of high $\kappa$-materials

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1 Introduction

Microelectronics has undergone an enormous development in recent years with an ever increasing performance of integrated circuits. This development has been made possible by modern CMOS technology, notably the down-scaling of transistor dimensions that leads to an exponentially increasing number of transistors on a chip, known as the famous Moor’s law. However, in the very near future continuing the down-scaling will become difficult due to a number of issues resulting in excessive power consumption and heat generation of integrated circuits. Therefore, the semiconductor industry is looking for alternative performance boosters, in particular by introducing new materials into the traditional, standard silicon CMOS technology encompassing new source/drain as well as channel materials. One of the most promising approaches is the replacement of bulk-silicon as the active channel material with strained silicon-on-insulator (sSOI). Strained silicon exhibits an electron mobility twice as high as bulk silicon. A higher mobility translates into a larger drive current in field-effect transistors and hence allows for faster chips without scaling. In addition, sSOI can easily replace SOI without many changes in the production technology since basically the same materials are being processed as in the SOI case.

Another new class of materials, which has to be introduced in advanced CMOS-processing, are the high-$\kappa$ gate dielectrics. For the thickness of the standard gate SiO$_2$ based gate dielectric drops below the tunnelling limit, gate leakage increases tremendously when the devices are scaled down further. To prevent tunnelling currents physically thicker dielectric layers are requested, but the electrical behavior of the MOS-Capacitor has to be maintained. To compensate the electrical differences when the layer is physically thicker, the $\kappa$ of the material has to be higher.

A whole zoo of materials as HfO$_2$, ZrO$_2$, rare earth scandates and LaLuO are under investigation to check their application suitability.

2 The Metal Oxide Semiconductor Field Effect Transistor

In this section the layout and functionality of a MOSFET will be described briefly, a detailed treatment can be found in [1, 2].

2.1 The MOS-Diode

The MOS diode consists of a metal layer (M), an oxide (O) and a semiconductor (S) (Fig. 1.a). In the ideal case the band alignment at the interfaces is as depicted in Fig.1.b for a n-doped semiconductor. In the semiconductor the Fermi-Level $E_F$ is shifted by $E_B = kT \cdot \ln \frac{n_{eq}}{n_i}$ from the intrinsic level $E_{Fi}$. Here $n_{eq}$ is the equilibrium concentration of electrons in the n-doped semiconductor and $n_i$ the intrinsic carrier concentration. By applying a voltage to the MIS-diode a potential $\psi(x)$ is induced, causing the carrier concentrations to be changed.

For the carrier concentration the following equations hold:

\[
\begin{align*}
n_n(x) &= n_{n0} \exp \left( \frac{q\psi(x)}{kT} \right) \\
p_n(x) &= p_{n0} \exp \left( -\frac{q\psi(x)}{kT} \right)
\end{align*}
\]
Fig. 1: a: MOS-diode; b: Bandalignment of the ideal MOS-diode at flatbandvoltage; $q\Phi_s$, $q\Phi_m$ work function in the semiconductor and the metal, respectively, $\Phi_B$ volume potential and $E_C$, $E_V$ conduction band edge and valence band edge of the semiconductor.

$n_n$ is the concentration of electrons and $p_n$ the concentration of holes in the n-type semiconductor. If $\psi(x) > 0$, the band edges will be lowered and the electron concentration increases. Assuming the interface between semiconductor and oxide at $x = 0$, then $\psi_S = \psi(0)$ is the interface potential and $n_S$ and $p_S$ are the carrier concentrations at the interface.

If a voltage is applied, the following cases can be differentiated: ([2], S. 362 ff):

1. $\psi_S > 0$: At the interface the bands bend down. The Fermi-level $E_F$ keeps constant, but the carrier concentrations change according to equations 1, 2. At the interface electrons - the majority carriers - accumulate. This case is called accumulation.

2. $\psi_S = 0$: The potential, and hence the band bending, is zero. The bands are flat and therefore this case is called flat band and corresponds to the ideal MOS-diode without applied voltage (cnf. Fig. 1).

3. $-\frac{E_B}{q} < \psi_S < 0$: By the band bending the free carriers were driven away from the interface and the region next to the interface is depleted (from free carriers). The ionized donator atoms form the space charge region at the interface. This case is called depletion.

4. $\psi_S = \frac{E_B}{q}$: The Fermi-level at the interface equals the intrinsic Fermi-level. Here the concentrations of free electrons and holes are equal. According to 1, 2 and $E_B = kT \ln \left( \frac{n_{i0}}{n_i} \right)$ the following equations hold:
\[
\begin{align*}
n_S &= n_n 0 \exp \left( \frac{E_B}{kT} \right) = n_i \\
p_S &= p_n 0 \exp \left( -\frac{E_B}{kT} \right) = \frac{p_n 0 n_n 0}{n_i} = n_i
\end{align*}
\]

This case is the onset of weak inversion.

5. \( \psi_S < -\frac{E_B}{q} \): With further decreasing \( \psi_S \) the concentration of the electrons, which actually are the majority carriers in an n-type semiconductor, drops below the concentration of the holes, the minority carriers. This state is called inversion, because at the interface the minority carrier concentration is higher than the majority carrier concentration, and the region at the interface is called inversion layer.

6. \( \psi_S < -2 \frac{E_B}{q} \): At \( \psi_S = -2 \frac{E_B}{q} \) the interface reaches strong inversion. The voltage, which has to be applied to reach strong inversion is the threshold voltage \( V_{th} \). A further increase of the voltage applied will not change \( \psi_S \) because the change in the voltage will be screened by the inversion layer.

For p-type semiconductor similar arguments hold. Here the inversion layer will be formed by electrons and not by holes.

In a MOS-diode the carrier concentration at the interface between semiconductor and oxide can be changed from accumulation of majority carriers to an accumulation of minority carriers by applying a voltage across the device. This field effect is the working principle of the MOSFET. In a real MOS-diode there is a difference in work function \( \phi_m - \phi_S \) between metal and semiconductor and there are carriers in the oxide \( Q_{ox} \) and at the interface \( Q_{it} \). Therefore at zero voltage there will be a band bending. The voltage, which has to be applied to reach flat band conditions, is the flat band voltage \( V_{fb} \).

The interface carrier concentration \( Q_{it} \) depends on the interface state density \( D_{it} \). Applying a voltage at the MOS-diode shifts the fermi-level \( E_F \) in respect to the valence and conduction band edges. During this shift interface states are charged or discharged, when \( E_F \) drops below the energetic level of the states, which leads to a change in \( Q_{it} \). This results in a different potential at the interface, and hence to the shift of threshold voltage \( V_{th} \).

Therefore the materials chosen to fabricate a MIS-diode or a MOSFET have to be bear low work function difference and a low interface state density.

### 2.2 The MOSFET

After depicting the the MOS-diode and the mechanism of the inversion layer, the MOSFET is explained. In Fig. 2 a MOSFET is shown schematically. The device has three terminals, the source, the drain and the gate, and consist out of two pn-junctions, connected back to back, and a MOS-diode. Between the two pn-junctions a barrier is formed, which prevents current flow from source to drain. By applying a voltage \( V_{gs} \) between the gate, the metal of the MOS-diode, and the source, at the interface between oxide and semiconductor the barrier is lowered by the field effect. When inversion is reached, a conducting channel is formed between source and drain, whichs conductance can be controlled by the gate voltage \( V_{gs} \). Depending on which type of carriers will form the channel, n-channel (electrons) and p-channel (holes) MOSFETS are distinguished.
2.2.1 Device characteristics and performance parameter of a MOSFET

In this section the device characteristics are explained. A mathematical treatment can be found in [1, 2]. Here only the fundamental contexts are presented. Therefore the following assumptions are made.

1.: An ideal MOS-diode is present
2.: The carrier mobility $\mu$ is constant
3.: The channel doping is homogeneous
4.: In the channel the electric field $E_x$ perpendicular to the channel is much larger than the electric field $E_y$ parallel to the channel

This gradual channel approximation allows us to use an one-dimensional mathematical formalism when describing the MOSFET behavior. There are two types of device characteristics of importance for describing the MOSFET behavior. The output characteristics, showing the drain current $I_d$ versus the source-drain voltage $V_{ds}$ with the gate voltage $V_{gs}$ as parameter, and the transfer characteristics, showing $I_d$ versus $V_{gs}$ with $V_{ds}$ as parameter.

2.2.2 Output characteristics

In Fig. 3 the output characteristics are shown schematically. There are two regions: The linear region (region I in Fig. 3) and the saturation region (region II).

In the linear region the drain current $I_d$ increases parabolically with source-drain voltage $V_{ds}$. For small $V_{ds}$ the increase in current can be approximated by a straight line. The inversion channel is formed across the whole gate-length $L_g$ and results in an ohmic resistance between source and drain (cnf. Fig. 4.a). The drain current $I_d$ obeys the formula [2]:

$$I_d = \frac{W_g}{L_g} \mu C_{ox} (V_{gs} - V_{th}) V_{ds}$$  \hspace{1cm} (3)

$\mu$ is the carrier mobility, $C_{ox}$ capacitance per area, $W_g$ the channel width, $L_g$ the channel length and $V_{th}$ the threshold voltage. The device behaves as a controllable ohmic resistance.
Fig. 3: Schematic view of the output characteristics of a MOSFET. $I_d$ is plotted versus $V_{ds}$ with $V_{gs}$ as parameter.

Fig. 4: MOSFET in on state for different $V_{ds}$. 
When $V_{ds}$ increases, the potential at the drain side of the channel changes. At a certain source-drain voltage $V_{ds}$, the saturation voltage $V_{ds,sat}$, the inversion layer at the drain vanishes (cnf. Fig. 4.b): the channel is pinched off. From this $V_{ds}$ the drain current keeps constant ([2] S. 442):

$$I_{d,sat} \sim \frac{W^2}{L_g} C_{ox} (V_{gs} - V_{th})^2$$

(4)

The saturation current $I_{d,sat}$ is constant, because the voltage drop between source and the pinch off point keeps constant. At the pinch off point the carriers will be injected into the not inverted channel region and will follow the electric field toward the drain.

### 2.2.3 Transfer characteristics

In Fig. 5 the transfer characteristics of a MOSFET is shown schematically. It can be divided into three regions: The off region (region 1; cnf Fig.5), the subthreshold region (region 2; cnf Fig.5), where the transistor is switching on and in the on region (region 3; cnf Fig.5).

The transistor is switched off, when no channel - no inversion layer - is present. The MOS-diode is in depletion. The only current flowing is the leakage current $I_{off}$. In the subthreshold region the MOS-diode is in weak inversion and the drain current $I_d$ increases exponentially with $V_{gs}$ [2]. In the on region, the current is independent of $V_{ds}$.

### 2.2.4 Parameter

A measure for the ability of the MOSFET to switch from off to on is the subthreshold slope $S$. It is the reciprocal gradient of the transfer characteristic in the subthreshold region and is measured in $mV/\text{decad}$. When the gradient in the subthreshold region is small, $S$ is large and a larger

![Diagram](image_url)
voltage range is needed to increase the drain current by 1 decade. This means that the operating voltage of the circuit has to be larger, too. A transistor with a small $S$ can be switched on and off more easily. There is a theoretical limit of $70 \mu V_{dec}$ as lower boundary for $S$.

The transconductance $g$ is the derivation of the transfer characteristics (cf. 5). It can be normalized to the gate width $W_g$ ($g_m$)(cfn.6). The transconductance is a measure for how many current can be gained, when the gate voltage is increased. For conventional planar devices $g$ is:

$$ g = \left. \frac{\partial I_d}{\partial V_g} \right|_{V_{ds}=const} \sim \frac{W_g}{L_g} C_{Ox} \sim \frac{W_g}{L_g \cdot d_{Ox}} \quad \text{mit } V_{ds} \geq V_{ds,sat} \quad (5) $$

$$ g_m = \frac{g}{W_g} \sim \frac{1}{L_g \cdot d_{Ox}} \quad (6) $$

In the linear region the drain current can be described by

$$ I_d = \frac{W_g^2}{L_g} \mu C_{Ox} (V_{gs} - V_{th}) V_{ds} \quad (7) $$

so the transconductance is:

$$ g = \frac{W_g}{L_g} \mu C_{Ox} V_{ds} \quad (8) $$

In the on region the saturation current $I_{d,sat}$ is:

$$ I_{d,sat} = \frac{2W_g}{L_g} \mu C_{Ox} (V_{gs} - V_{th})^2 V_{ds} \quad (9) $$

and:

$$ g = \frac{4W_g}{L_g} \mu C_{Ox} (V_{gs} - V_{th}) \quad (10) $$

## 3 High-κ gate oxides

### 3.1 The evolution of high-κ dielectrics

The desired down-scaling and performance enhancements of CMOS-devices require the replacement of silicon dioxide as gate dielectric. The reason is simple: the thickness of SiO$_2$ already reaches a critical value of about 1 to 2 nm. Using even thinner SiO$_2$ is an advantage with respect to an increase of the oxide capacitance $C_{Ox}$ at first sight: The effect of a higher capacitance $C_{Ox}$ can be directly seen in the equations of the MOS-diode introduced in the previous section. But the isolating character of these thin films is limited to a certain critical thickness and as a consequence high leakage currents and power dissipations are present reaching these regime. Replacing SiO$_2$ by a material with a higher dielectric constant $\kappa$, so called high-κ dielectrics, could overcome these problems. Due to the proportionality of the dielectric constant $\kappa$ to the capacitance, they provide directly a higher capacitance in comparison to the equivalent SiO$_2$-thickness. Looking for adequate candidates to replace silicon dioxide SiO$_2$, which matches as native oxide perfectly to Si, is not that easy. One of the first approaches to increase the $\kappa$-value was to 'add' nitrogen to the SiO$_2$ forming so called silicon oxynitride, SiO(N), films. But simulations and first experimental tests highlight more promising oxides
based on rare-earth compounds. To fully integrate them as alternative oxides the following requirements have to be satisfied:

- thermal stability (up to 1000 °C)
- sufficient band offset $\geq 1 \text{ eV}$, band gap $\geq 5 \text{ eV}$
- dielectric constant value much higher than SiO$_2$ but smaller than 60 (to avoid ferroelectrical effects)
- compatibility with CMOS-technology and -materials
- stable morphology, preferentially amorphous
- high quality of high-$\kappa$/Si-interface
- reliability

An overview of these candidates is given in figure 6 and in table 1. One might query whether it is realistic to have MOSFETs with such exotic gate oxides in the future. Intel already resolves all these doubts by introducing 2008 hafnium oxide HfO$_2$ into their fabrication process of microprocessor devices.

**Fig. 6:** Band gap vs static dielectric constant ($\kappa$) for candidate high-$\kappa$ gate oxides. Modified from [7].
<table>
<thead>
<tr>
<th>material</th>
<th>κ-value</th>
<th>thermal stability</th>
<th>$E_g \pm 0.1$ [ev]</th>
<th>$E_C \pm 0.1$ [ev]</th>
<th>$E_V \pm 0.1$ [ev]</th>
</tr>
</thead>
<tbody>
<tr>
<td>GdScO$_3$</td>
<td>23</td>
<td>$\leq 1000 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>DyScO$_3$</td>
<td>23</td>
<td>$\leq 1000 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>TbScO$_3$</td>
<td>26</td>
<td>$\leq 1000 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>LaScO$_3$</td>
<td>28</td>
<td>$\leq 800 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>SmScO$_3$</td>
<td>29</td>
<td>$\leq 800 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>LaLuO$_3$</td>
<td>30-32</td>
<td>$\leq 1000 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.1</td>
<td>2.1</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>23-32</td>
<td>$\leq 550 , ^{\circ}C$</td>
<td>5.6</td>
<td>2.0</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Table 1: Dielectric constant ($\kappa$), optical band gap ($E_g$), conduction ($\Delta E_C$) and valence ($\Delta E_V$) band offsets to silicon, for amorphous films of the scandates, LaLuO$_3$ and HfO$_2$. The κ-values were extracted from EOT plots. The energy band parameters were determined using a combination of internal photoemission and photoconductivity measurements. From [6].

### 3.2 Electrical properties

In order to analyse the properties of such new gate stack designs, which is the combination of high-$\kappa$ and an appropriate metal, we have to find a quick and reliable method: An important fingerprint of the characteristics of those structures is given by the curvature of a capacitance measurement versus voltage of the MOS-diode, a so-called C/V-measurement. It’s performed by applying on a gate stack a superposition of a bias-voltage and a low-amplitude AC-voltage (typically 50 mV). The AC-current at each bias-voltage gives the capacitance at each voltage. The voltage sweep goes from negative to positive voltage and from positive to negative. This measurement method ensures that possible hysteresis effects can be identified.

![Fig. 7: C/V-Measurement of a Al/TiN/HfO$_2$/Si-MOSCAP structure. The voltage is applied to the top electrodes.](image)

Applying a negative gate voltage leads the semiconductor to the accumulation regime. The
majority charge carriers are near the oxide/silicon interface and the capacitance of the gate stack is dominated by the oxide capacitance. By reducing the gate voltage in an ideal MOS-diode the flat band voltage is reached at 0 V. In our case the inflection point indicates the flat band voltage. Applying a positive gate voltage two possible cases can be observed, depending on the frequency of the superimposed AC-voltage. If the AC-voltage is low, the semiconductor will stay in an inversion state: Minority carriers will accumulate at the interface capacitance leading to an increase of the capacitance until the value of the oxide capacitance is reached. In case the frequency is too high, the minority carriers cannot follow the changes of the electrical field and no inversion layer is formed. The semiconductor stays depleted. In figure 7 only the latter case is shown.

The orientation of the C/V-measurement gives the type of dopant in the semiconductor and from curvature the strength of the doping can be extracted. The higher the semiconductor doping concentration, the higher is the capacitance of the capacitor in depletion.

Moreover, it is possible to extract from the C/V-measurement the type and number of defects at the interface and in the oxide. Fixed charges in the oxide can move the C/V-curve along the x-axis which is the same as a flat band voltage shift. Depending on the polarity, this can result in a shift to a positive or negative voltage. Interface trapped charges create an additional slope between depletion and accumulation and this effect is called stretch out. Mobile charges are responsible for a so-called hysteresis effect in the C/V-measurement.

To have access to these different properties, an additional point has to be taken into account. Working with SiO$_2$, no interfacial layer has to be considered in a capacitance-measurement of a MOS-capacitor. The capacitance can be calculated just by using the simple formula:

$$C_{OX} = \epsilon \epsilon_0 A / d$$  \hspace{1cm} (11)

$A$ is the area of the capacitor, $d$ is the thickness of the oxide and $\epsilon$ and $\epsilon_0$ are the dielectric constant of SiO$_2$ and of the vacuum, respectively. The equivalent oxide thickness $t_{eq}$ of the high-$\kappa$ layer is easily calculated using:

$$t_{eq} = \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} t_{high-\kappa}$$  \hspace{1cm} (12)

while $\kappa_{SiO_2}$ is the dielectric constant of the SiO$_2$, $\kappa_{high-\kappa}$ the dielectric constant of the material and $t_{high-\kappa}$ its thickness. Unfortunately, adding another oxide in a gate stack normally leads to the growth of an interfacial layer between silicon and oxide.

![Fig. 8](image.png)

**Fig. 8:** Scheme of a real structure of a gate stack with a high-$\kappa$ dielectric layer. A series capacitance has to be taken into account to evaluate the dielectric constant of the high-$\kappa$ material.

As a consequence, this interfacial layer has to be considered during the characterization. This is done in a so-called CET-plot (CET = capacitance equivalent thickness) or EOT-plot (EOT =
equivalent oxide thickness). The empirical relation between CET and EOT is given simplified by

\[
\text{CET} - 0.3 \text{ nm} = \text{EOT} \quad (13)
\]

This 0.3 nm thickness reduction is the contribution due to quantum mechanical effects. To generate a CET- or EOT-plot, capacitors, each one containing a high-\(\kappa\) oxide film of a different thickness, have to be prepared and the measured capacitance plotted versus the real thickness of the high-\(\kappa\) film. The real thickness can be determined, e.g. by ellipsometry in the clean room. Doing so, the following calculation has to be performed. The thickness of the oxide in the MOS-structure is

\[
d_{\text{ges}} = d_{\text{SiO}_2} + d_{\text{high-}\kappa} \quad (14)
\]

The corresponding capacities for the \(\text{SiO}_2\)-layer and the high-\(\kappa\)-film are listed below. Putting

\[
C_{\text{SiO}_2} = \epsilon_0 \cdot \epsilon_{\text{SiO}_2} \cdot \frac{A}{d_{\text{SiO}_2}} \quad \quad C_{\text{high-}\kappa} = \epsilon_0 \cdot \epsilon_{\text{high-}\kappa} \cdot \frac{A}{d_{\text{high-}\kappa}} \quad (15)
\]

all together in the formula for capacitors in series one end up with

\[
\frac{1}{C_{\text{ges}}} = \frac{1}{C_{\text{SiO}_2}} + \frac{1}{C_{\text{high-}\kappa}} \quad \quad C_{\text{ges}} = \epsilon_0 \cdot \epsilon_{\text{SiO}_2} \cdot \frac{A}{d_{\text{CET}}} \quad (16)
\]

\[
\frac{d_{\text{CET}}}{\epsilon_0 \epsilon_{\text{SiO}_2} A} = \frac{d_{\text{high-}\kappa}}{\epsilon_0 \epsilon_{\text{high-}\kappa} A} + \frac{d_{\text{SiO}_2}}{\epsilon_0 \epsilon_{\text{SiO}_2} A} \quad (17)
\]

\[
d_{\text{CET}} = \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{high-}\kappa}} d_{\text{high-}\kappa} + d_{\text{SiO}_2} \quad (18)
\]

d_{\text{CET}} is linearly dependent on the \(d_{\text{high-}\kappa}\) and \(d_{\text{CET}}\) gives for \(d_{\text{high-}\kappa}=0\) the thickness of the interfacial layer in the structure. It can be directly seen that the dielectric constant \(\kappa\) can be extracted by plotting the EOT vs the real thickness (measured e.g. by ellipsometry).

**Fig. 9:** (Left) Illustration of extracting the parameters out of a CET-plot. (Right) EOT plot for amorphous LaLuO\(_3\) films deposited by MBD at 450 °C.
4 Device Fabrication

The fabrication of the devices will be carried out in the central clean room facility of the PGI. All participants have to wear a full cover with hoods, gowns and boots. The advisor will instruct the participants how to dress and how to behave in the clean room. Since the work will be done in the central facility great care has to be taken. In particular contamination is a severe issue and therefore the participants have to wear gloves at all times when being in the clean room. Protective clothing such as apron, a second pair of gloves with sleeves and a face shield is mandatory when working with hazardous chemicals.

Each participant will get a sample which is fortified with a aluminum layer on the backside of the wafer. On the front side there are HfO\(_2\) layers with varying thicknesses (sample A: 8.6nm, B 13.8nm and C 18.0nm) and a 20nm TiN capping layer (Fig. 12.a). The fabrication is listed below. In addition, the participants will be handed out clean room paper (a special, particle-free paper) to protocol the fabrication process. Take as many notes as necessary since this will be attached to the written report as an appendix.

![Control panel of hot plate](image)

**Fig. 10:** Control panel of hot plate: 1 Main switch; 2 START; 3 STOP; 4 time controller; 5 temperature controller

4.1 Process flow

- **Prepare wet bench for resist coating:**
  - Set temperature of right hot plate to 110°C and 1 minute process time (Fig. 10): press upper set key, use arrow keys for temperature adjustment. Press lower set key and adjust time to 1 minutes.
  - Set VPO to process parameters: switch on Vacuum Pump (key next to VPO-controller). Select ”Betriebsart” AUTO, press E (Fig. 11); Choose recipe: press 1, confirm with E.
Fig. 11: Control panel of resist coater and VPO: 3.1 display, 3.2 Vacuum toggle, 3.3 level-up/down key, 3.5 START/STOP process, 3.6 key pad, 3.8 E-key

- Set resist coater to process parameters (Fig. 11): select ”Betriebsart” AUTO, press E. Choose recipe 4 by pressing 4, confirm with E. Adjust chuck for 2cm * 2cm samples on spinner.

**Apply resist to samples:**

- dehydration of the samples at 110°C for 5 minutes: place samples on right hot plate, blow clean with nitrogen and press start. Wait process time.

- apply primer HMDS with VPO: place sample on VPO-Plate, blow clean with nitrogen and close cover. Press START; in the display appears the question, if the lid is closed; confirm with START. Wait process time. Remove sample and confirm with E.

- Apply photo resist (AZ n-lof 2020) spin-on at 4000 rpm: place sample on chuck, blow clean with nitrogen, apply resist, close cover and press START. After spinning confirm with E

- pre-bake on a hot plate at 110°C for 1 minute: place sample on right hot plate and press START; wait process time (Fig. 12.b)

**Exposure with mask-aligner 3: expose samples with 2.84 mJ/cm².**

- Adjust exposure time: Press ”Lamp Test” and read light intensity from CIC2000; calculate exposure time. Press ”lamp test” again. Press ”edit parameter” and adjust exposure time.

- Chose contact mode: Chose ”hard contact” by pressing ”program edit” until ”hard contact” is displayed on the screen.

- Mount mask to mask holder: Press ”change mask” and remove mask holder, Fix mask on holder and toggle vacuum by pressing ”enter”. Place mask holder back on aligner.
Fig. 12: Schematic view of the process flow

- Mount chuck: Pull slide out, mount $2\text{cm} \times 2\text{cm}$-chuck, blow clean with nitrogen.
- Load sample: Press "load"; pull slide and place sample on chuck, confirm with "enter". Blow sample clean with nitrogen, push slide back, confirm with enter. The tool will bring sample and mask into contact and after wedge error correction separates both by 40m (the single steps will be displayed on the screen).
- Align sample to mask: Use manipulators for x-, y- and $\theta$-adjustment.
- Exposure: press "exposure". After exposure, the chuck will go down again.
- Unmount sample: pull slide and unmount sample. Follow the instructions on the screen.

**Development:**

- Post exposure bake: to enhance exposure, a so called post exposure bake (PEB) has to be done at $110^\circ\text{C}$ for 1 minute. Place sample on right hot plate and wait process time.
- Development: develop in undiluted MIF326 for 75s, rinse thoroughly in DI-water (Fig. 12.c)

**Metallization**

- Aluminum evaporation: samples are mounted into an e-beam evaporation chamber and aluminum (150nm) is deposited. Prior to evaporation the samples where insitu AR-sputtered for 5s (Fig. 12.d).
- Lift-Off: put samples in acetone. The solvent will solve the resist and the metal on top will be removed from the sample.
- After lift-off, rinse in propanol and blow dry with nitrogen (Fig. 12.e)
• TiN patterning and anneal

  – Etching of TiN: the Aluminum contact pads are used as etching mask to pattern the TiN layer by reactive ion Etching (RIE).

  – After TiN etching do post metallization anneal (PMA). Mount samples into RTP furnace 3 and run recipe 450-15 (10 minutes forming gas (90% N₂:10% N₂) at 450°C (Fig. 12.f).

Fig. 12 shows a schematic overview of the process: a) the sample with the HfO₂ and TiN layer, b) after resist application, c) after development, d) after Al evaporation, e) after lift-off and e) shows the sample after finishing the process by removing the TiN layer.

5 Measurement Setup

5.1 Determination of the pad area with an optical microscope (Optional)

Depending on the quality of the sample fabrication, i.e., lithography and lift-off process the nominally desired values of the contact pad dimension will not be reached exactly. For the normalisation of the capacitance the actual values of the pad area are therefore better. With the help of an optical microscope it’s possible to take pictures of the structures. Due to the contrast between Al-contacts and substrate, the pad regions can be identified by a small LabVIEW-program. By typing in the zoom factor, identifying the different colours and mark the region, the program calculate directly the area.

Fig. 13: Determination of the pad area by using a LabVIEW program to identify contrast regions of the optical microscope images

5.2 C/V measurement

The C/V-measurements will be performed with a 2-terminal measurement setup. Two tungsten needles can be placed carefully on the Al-contacts. One is marked with L for LOW, the other with H for HIGH voltage. HIGH means that here the voltage is applied. It’s better to apply the voltage to the large contact pad of our MOSCAP structure to ensure the best result. The two tips can be moved precisely by using the adjusting screws. The microscope helps to contact the MOSCAP contact pads with the tungsten needle. The tip is in contact with the pad if the needle moves a little bit forward while moving it carefully down. An HP 4192A LF Impedance Analyzer is directly connected with the probe arms and the measured values are plotted and listed with a self-written and intuitive LabVIEW-program called ’CV-MOS v6’ which provides...
all necessary setting options, like range, delay time, frequency and more. By pressing the button 'CV-measurement': capacitance, conductivity and dissipation versus voltage are measured and plotted simultaneously. Another option is to make a frequency dependent CV-measurement: C/V-curves for 1 kHz, 10 kHz, 100 kHz and 1 MHz are recorded in a row. The measured curves can be saved in the lab folder to analyse them later in Origin etc. The program tries to fit these curves with a calculated model directly. To ensure that the values which are extracted out of fitting the curves, e.g. flat band voltage $V_{FB}$ and capacitance equivalent thickness $CET$ are correct, one have to set the correct pad area and the right magnitude of doping concentration of the p-doped Si wafer in advance.

![Fig. 14: C/V measurement program](image)

### 5.3 Karl SUSS Probe System

The leakage current of the devices will be determined with a manual Karl SUSS probe system PM 5 in combination with a Keithley 4200-SCS (semiconductor characterisation system). The Karl SUSS Probe System PM 5 which is shown in figure 15 has four probe heads with tungsten needles. Only one of them will be used to contact the MOSCAP. The backside of the sample, the Al-contact, is placed in the middle of the chuck and fixed by applying a vacuum to the sample. To put the wafer onto the chuck the whole chuck has to be pulled out with caution by simultaneously pressing the small lever and pulling the handle at the front side of the chuck. After putting the chuck back, it has to be raised using the small lever arm in front of it on the right side. To adjust the needles, the probe heads allow independent X, Y and Z travel. Additional movement of the chuck and the microscope in plane is possible with the knobs on the right side of each, the chuck and the microscope.
Fig. 15: *Probe System PM 5*

5.4 **Keithley Semiconductor Characterization System**

The Keithley Semiconductor Characterization System 4200 is an electronic instrument for measuring and analyzing the characteristics of semiconductor devices. It provides two types of measurement, sweep measurements and sampling measurements, whereas for the characterization of the MOSCAP, only sweep measurements are used here. For the measurement a template of a MOS-diode structure in the KITE (Keithley Interactive Test Environment) can be used. This template is depicted in Fig. 16. After assigning the SMUs (Source Measurement Unit) to the corresponding chuck (Anode) and tip (cathode) connector, the voltage sweep can be defined by pressing the 'Force Measurement'-button.

Fig. 16: *Electrical measurement setup for the determination of the leakage current.*

The window depicted in Fig. 17 appears, where the properties of the voltage sweep can be set
in detail.

![Voltage Sweep Settings](image)

**Fig. 17: Voltage Sweep Settings.**

Finally the measurement starts by pressing the green arrow in the upper bar. By clicking the tab 'Sheet', you can observe that the measured values are written in a tabular with the columns, applied bias voltage and leakage current. With a mouse click on the tab 'Graph' these values are visualized in a plot. Often it’s necessary to scale the axis and define the display properties after the measurement to see the actual curve. The button 'Graph settings' serves these functionalities.

6 Electrical Measurement and Characterization

Depending on the mask used the design parameters of the MOSCAPs can be provided by the tutor. The following measurements and characterizations are to be made:

- Determine the real area of the structure by using an optical microscope (Optional)
- Measure (for all wafer types) the capacitance versus bias voltage (C/V measurement) in an appropriate gate voltage range. Plot the C/V curve with and without the area normalisation of the capacitance against the bias voltage. Try also different geometries and area sizes.
- Measure (for all wafer types using the same pad size) frequency dependent C/V curves of 1 kHz, 10 kHz, 100 kHz and 1 MHz.
- Measure (for all wafer types) the leakage current versus the backside contact bias voltage.
- Extract out of the measurements $C_{ET}$, $V_{FB}$, $\kappa$ by analysing the plots C/V, EOT vs real thickness and try to interpret all the measured curves with respect to frequency/area/geometry dependencies.

After the characterization each group is supposed to write a short report. Since writing reports is often considered as being boring you should write it with the following background: You work for an up-and-coming company developing alternative gate oxides and have been called by the CEO of a foundry that has been producing gate stacks with standard...
gate oxides since its foundation. The CEO has only a limited technical background but has to decide between several technology options. To improve the performance of the company’s transistors he could either move ahead with the common gate oxides implying a severe financial investment. On the other hand he heard about the option using the alternative high-$\kappa$ but he does not know much about this new technology. Being a representative of your company you should convince the CEO of replacing the conventional SiO(N)-based oxides:

- Write a cover letter stating your recommendation, the key benefits of replacing the SiO(N) with high-$\kappa$-dielectrics and pointing out to the enclosed material that backs up your recommendation (the technical annex). Remember that the CEO has only a limited technical background. Therefore, the style of the letter should be a mixture of business- and technical-like. But most of all it should be convincing! It’s your company that needs this big contract. (You might want to use this opportunity to give your company a fancy name.)

- Prepare a technical annex. In this annex you should explain and show the MOSCAP results. You should also state and explain shortly the method you used to obtain the data. To this annex your lab notes should be added. Refer to these notes in the technical annex.

- Have fun!

References


