# Thesis Project Offer

**Joint Research and Education Programme “Palestinian-German Science Bridge PGSB”**  
Forschungszentrum Jülich GmbH & Palestine Academy for Science and Technology

## Thesis type*

| ☐ | □ | ☒ | ☐ | ☐ |

| BSc | MSc | PhD | Intended starting date (approx.): flexible |

## Contact details of supervisor/responsible host at Forschungszentrum Jülich

<table>
<thead>
<tr>
<th>Title*</th>
<th>Degree</th>
<th>First name*</th>
<th>Surname*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mr.</td>
<td>Degree Dr.</td>
<td>Michael</td>
<td>Schiek</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phone*</th>
<th>E-mail*</th>
</tr>
</thead>
<tbody>
<tr>
<td>+49246161-2516</td>
<td><a href="mailto:m.schiek@fz-juelich.de">m.schiek@fz-juelich.de</a></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Function*</th>
<th>Institute and homepage of institute*</th>
</tr>
</thead>
</table>
| Scientific Staff | Central Institute of Engineering, Electronic Systems –Engineering and Technology (ZEA-2)  
www.fz-juelich.de/zea/zea-2/ |

## University affiliation in Germany*

Duisburg-Essen

## Co-Supervisor at Palestinian university (if applicable)

<table>
<thead>
<tr>
<th>Title</th>
<th>Degree</th>
<th>First name</th>
<th>Surname</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Degree</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phone</th>
<th>E-mail</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>University/institution</th>
<th>Department/faculty/institute</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Project description*

**Verification of chip prototypes**

ZEA-2 is engaged in the development of complex, modular and high-scale cross-linked measurement, detector and sensor systems. Hereby the preferred approach are silicon-based System-on-Chip (SoC, highly integrated) solutions.

This approach requires a thoroughly verification of the developed prototypes for which a modular MATLAB based automated verification framework has to be developed. According to the different chip developments and application specific adaptions of the complete system this verification framework has to be successively extended over the next years.

In this context the master theses shall concentrate on the development of automated test scenarios including parameterized generation of test signals, analyzing system’s response and interfacing the software with the testing PCB and special verification equipment like logic analyzers and digital oscilloscopes. The software development shall be done using MATLAB/SIMULINK including the corresponding toolboxes, in particular the ‘Real-Time’, ‘DAQ’ and ‘Control System’, and C/C++ for coding hardware specific interface routines.
Required skills/experiences:
• Electrical engineering background
• Modelling
• PCB design
• Digital signal processing
• MATLAB/SIMULINK
• C/C++

There is also an option of continuing work in the form of a subsequent PhD

Date*  Signature*
18.10.2017  M. Schult

* required field