Runsheet set up and what is its purpose

All activities which should be done in the HNF require a proposal, which is evaluated by the TechCom (hnf-technologie@fz-juelich.de) in advance of starting the work in the HNF. This is necessary for several reasons:

We would like to see what materials you intend to work with in the HNF. For there is a wide range of different materials and scientific topics there is also a wide range of materials and chemicals needed to cope with that task. Unfortunately often those materials interfere with each other. E.g. K and Na are a major drawback for Si device processing and every work, which depends on the electrical properties of Silicon; for samples on which cells should be cultivated after processing it is necessary to avoid contamination with As, Te or Bi.

Especially when you need new chemicals we have to know about that, because we have to fulfill safety requirements in the cleanroom and the HNF at all. There have safety measures to be taken to avoid harm to equipment and first and foremost people. In principle the same is true for tools.

Many processes are taken from literature. This is of course reasonable, but it is as well reasonable to adopt the single process steps to our technology. E.g.: In the literature there might resist XYZ be used to do a certain lithography. One of our standard resists often can replace this non-standard resist XYZ easily. The same is true for spin speed during resist coating: if the authors use 2500rpm this might be due to standards in their laboratory, but not for technological reasons; so our standard of 3000rpm might do, too.

To be able to assign your work to different tools, we have to know the sample size and why this size is chosen. There might be technical reasons that you have only samples of e.g. 7mm by 7mm size, but often we see, that it is possible to do some of the process steps with larger samples before the will be cut to small pieces.

So when you write your proposal, keep the following in mind:

- Which samples do you have (size/material)
- Which materials are on the sample
- Which materials have been on the sample and how have they been removed
- Which chemicals have been used to treat the sample before
- What is the aim of the single step in your process (e.g. resist coating for optical lithography for patterning structures of ~1µm times 10µm with RIE; etching depth ~500nm)
- Describe your process steps with as detailed as possible (temperatures, spin speeds, etc…); for new processes describe your aim and the means you want to obtain it.
- A sketch of the process is helpful (at least for longer flows)
- Do you need special chemicals for your purpose
- Do you need special tools

If you are not used to technology feel free to contact us before (hnf-technologie@fz-juelich.de), so we can help you to do develop the process flow and therewith the proposal.

On the next page you can see an example how a proposal should look like.

Realization of µ-apertures on Si_3N_4 membranes

Other people working on same or similar runsheet: Abel Kain, Karl Mustermann

Starting material: 100mm Silicon (100) wafers polished from both sides, vendor did clean wafers by 10nm thermal oxidation and HF etch.

1) Cleaning samples: Acetone/IPA/DI (WB2.1)
2) Marker definition: Lithography and subsequent etch of marker structures. Structure size several µm, etching depth ~500nm.
    a. Resist coating: UV26, 4000rpm (~1.7µm); Soft bake: 130°C, 60 s hot plate;
    b. Exposure: dose to be tested
    c. Post Exposure Bake: 110°C; 60s hot plate;
    d. Development: MF-24-A 60s
    e. RIE: anisotropic etching of 500nm of Si; side wall angle >75°
    JM-SF6/O2-LowT @ RIE 4 (SF6 40sccm, O2 8sccm, ICP 500W, RF 50W, T=120°C)
    f. Resist stripping: O_2-Plasma in RIE chamber
    g. Cleaning: H_2SO_4/H_2O_2 (2:1), 10 min, 60°C, Ultra Sonic
3) LPCVD: Deposition of 300nm Si_3N_4 (both sides)
4) Lithography backside: opening of Nitride mask on backside
    a. Resist coating: UV26, 4000rpm (~1.7µm); Soft bake: 130°C, 60 s hot plate;
    b. Exposure: dose to be tested;
    c. Post Exposure Bake: 110°C; 60s hot plate;
    d. Development: MF-24-A 60s
5) Etching of nitride mask: RIE of Si_3N_4 (CHF_3/CF_4)
6) Resist stripping: O_2-Plamsa in RIE chamber
7) Cleaning: H_2SO_4/H_2O_2 (2:1), 10 min, 60°C, Ultra Sonic
8) Wet etch of Silicon: etch vias through wafer
    a. HF-Dip: remove SiO_2 on Si with 1 min HF 1%
    b. KOH etch: etching of Si; time dependent etching; stop before Si_3N_4. Parameters to be clarified
    c. Remove Si_3N_4 from backside: RIE CHF_3/CF_4
    d. HF-Dip: remove SiO_2 on Si with 1 min HF 1%
    e. KOH etch: etch through wafer; stop on Si_3N_4 on front side. Parameters to be clarified
9) Deposit 30nm Au on front side
10) Deposit 30nm Au on back side
11) FIB: etch 2µm holes in Au/Si_3N_4/Au membrane

Kommentiert [MJ1]: When this is not a new runsheet, state this here. We can look those things up, which will speed up matters.

Kommentiert [MJ2]: Describe your samples. What is on those samples, what has been there and how was it removed. If layers are on the samples, where do they come from?

Kommentiert [MJ3]: When we had the same runsheet before, we did a tool assignment already. Include this in your runsheet.

Kommentiert [MJ4]: Give structure sizes

Kommentiert [MJ5]: name the resist; give parameters;

Kommentiert [MJ6]: For new processes this is standard. But when you have to update your runsheet (due to material or process flow changes), or when a new colleague starts on the same runsheet, update those items.

Kommentiert [MJ7]: Name the chemicals, give parameter

Kommentiert [MJ8]: If you know the recipe already, name it.

Kommentiert [MJ9]: Describe the process as detailed as possible

Schematic process flow

Kommentiert [MJ10]: This helps us to understand your process and helps us to give you advise, if necessary.