JARA-FIT

Nanoelectronic Lab Course

Alternative concepts for non-volatile memories

Peter Grünberg Institute – Electronic Materials

1) Introduction

Research in the field of random access memories (RAM) is concerned with three cardinal issues, true non-volatility (NV), speed, and extended scaling. The advent of a non-volatile memory with a high (Gbit) integration density would merge the advantages of today´s DRAM and mass storage devices, while stripping off the drawbacks. Especially as embedded memory, this would represent another revolutionary step in information technology, specifically in mobile applications and ubiquitous computing.

An ideal non-volatile memory comprises write and (preferably non-destructive) read operations at speeds comparable to those of logic devices, low energy consumption, infinite retention, and an infinite number of read and write cycles. A variety of physical principles has already been investigated in order to advance towards this ideal memory as far as possible. However, specific drawbacks are encountered in extended scaling of most concepts: Ferroelectric RAM (FeRAM) will suffer from geometrical limits to the scalability because of the required footprint area of (even highly folded) ferroelectric 3-D capacitors. Magnetic RAM (MRAM) requires an additional digit line and runs into current density as well as superparamagnetic effects on extended scaling. PCRAM (also called Ovonics RAM) shows relatively high energy consumption during write operations and may run into thermal cross-talk problems upon extended scaling. The challenge is to find a NV RAM which overcomes these and other potential drawbacks.

Another promising candidate for future non-volatile memories is the Resistive RAM (RRAM), based on materials which show a significant change in the resistance upon application of a voltage bias above a critical threshold and a switch back if polarized with the reverse voltage. The insulators are typically binary (TiO_2, NiO_2, WO_3), or ternary transition metal oxides, doped with other transition metal oxides, ($SrTiO_3$ or $Ba_xSr_{1-x}TiO_3$, doped with Mn, Cr, Fe). Even though these materials show promising properties, the involved switching mechanisms are still content of current research activities and the integration of these materials in RRAM architectures is in the early stage of development. Where the mechanism has been studied in depth, electrochemical reduction / oxidation (redox) process have been found. In the case of TiO_2, redox processes confined to dislocations as conductive paths were found to be responsible for the resistive switching.

In order to elucidate the mechanism of resistive switching in oxide materials and to clarify the suitability of these materials in future RRAM, one has to fabricate and characterize simple test cells, which are shown in Figure 1.

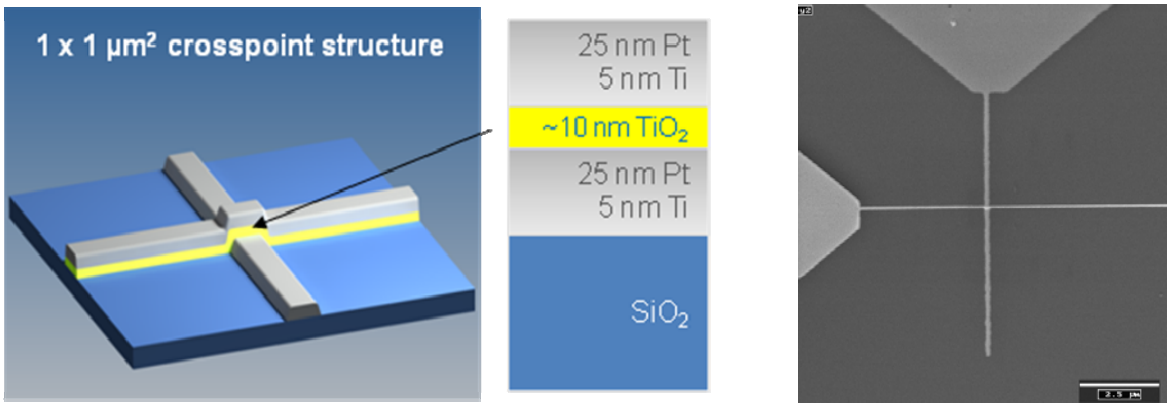


Figure 1: Simple crossbar test structure for electrical testing (schematic and top view under electron microscope).

2) Fabrication of test devices

The fabrication of the test devices can be roughly divided into the following steps:

1) Starting with a silicon substrate with structured Pt bottom electrodes
2) Deposition of the oxide thin film (e.g. TiO_2) by Atomic Layer Deposition (ALD)
3) Fabrication of a resist mask by photolithography which has to be aligned to the bottom electrode structure
4) Metallization and structuring of the top electrode by means of a lift-off technique.

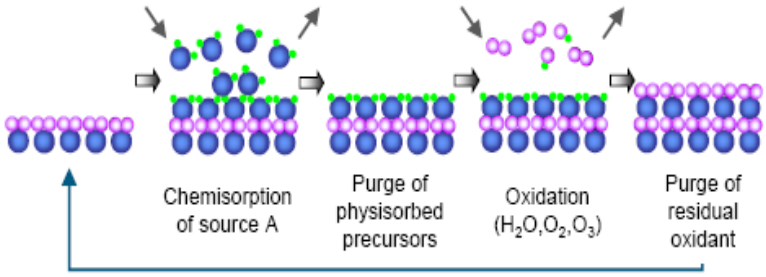
Metal thin films for the top electrode are deposited by either thermal or ebeam evaporation or they can be prepared by sputtering. Oxide thin films can be deposited by various techniques like sputtering, pulsed laser deposition (PLD) or by atomic layer deposition (ALD). Within this course, the oxide thin films will be grown by ALD and the metal films will be deposited by sputtering.

3) Thin film deposition by ALD

Atomic layer deposition (ALD) is a gas phase method based on alternate saturating surface reactions and the film growth is thereby self-limiting. In contrast to Chemical Vapor Deposition (CVD) where the precursor may react in the gas phase and is decomposed on the reaction surface, in the ALD process the precursor is chemisorbed at surface sites and any adsorbed molecules are removed in a purge process step. In a following step surface ligands

of the chemisorbed precursor molecules are exchanged against OH^- groups by offering a reactive gas. Therefore, ALD is a surface-reaction controlled process and thereby allows homogeneity and excellent film thickness controllability to be achieved on complex structures. ALD is one of the most important technologies in today's MOS gate oxide growth, DRAM and FLASH memory production. A comprehensive description of all details of the ALD technique and the involved chemical mechanisms can be found in Ref. [1].

The different stages of one ALD cycle are displayed in Figure 2:



1) Chemisorption of precursor molecules at surface sites;
2) Purge of physisorbed precursor molecules;
3) Oxidation of the chemisorbed species;
4) Purge of residual oxidant.

Figure 2: Principle of Atomic Layer deposition (ALD).

A schematic of the process flow for growth of multi component oxides is depicted in Fig. 3a. If all process steps are executed properly, the growth rate of the films saturates at a value with corresponds to the available surface sites, which means that any increase in precursor supply should not further increase the growth rate. The value depends besides others on the type of the substrate, the size and structure of the precursor molecule, and slightly on the temperature. The saturation behavior of the growth rate is shown in Fig. 3b.

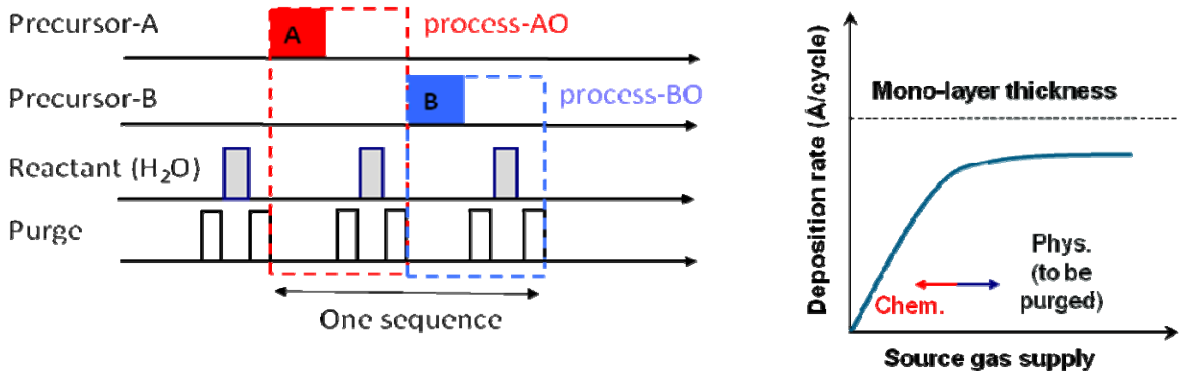


Figure 3: a) ALD process flow for multi component oxides, and b) a typical saturation dependence.

For substrate purposes, commercially available (100) oriented silicon wafers with a layer of about 400 nm thermal SiO_2 will be used cut into pieces of 1 x 1 inch^2. The Ti/Pt bottom electrodes were deposited by sputtering and were structured by means of photolithography and reactive ion etching. The ALD deposition of the thin TiO_x layer is performed in an ALD reactor which is equipped with a pulsed liquid injector. A schematic of the LI-ALD tool at PGI-7 is shown in Fig. 4. A dummy run for cleaning lines and reactor has been done prior to the deposition. The substrate is put on the susceptor disc and loaded to the reactor which is then evacuated to low pressure of about 10^{-2} hPa. Argon is flown through the reactor and the susceptor disc should rotate. At this state the susceptor is heated to the desired temperature (~250 °C). The valves of precursor bubbler and H_2O have to be opened and the ALD recipe has to be started on the computer. When the stable temperature is reached, the ALD routine will be automatically executed. In the liquid injection technique, the liquid precursor is sprayed into the vaporizer which is a heating tube with precise temperature control. The 'spraying' is done in pulses utilizing electromagnetic injectors from automotive applications. The process, i.e. opening and closing of the ALD valves within the different steps of an ALD cycle can be followed on the ALD control panel. For a TiO_2 film of 15 nm in thickness grown at about 250°C typically ~400 cycles are needed. When the process protocol is finished the substrate heater has to be switched off. The ALD valves have to be closed manually and the reactor pressure is set to atmospheric pressure by closing the valve to the pumping system and opening the venting valve to maximum. After atmospheric pressure is reached, all valves are closed and the sample is taken out.

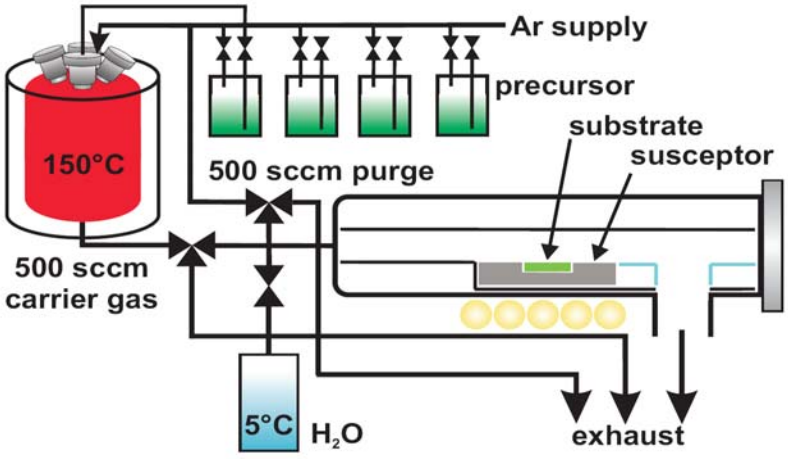


Figure 4: Drawing of the ALD system at PGI-7.

4) Photo-Lithography

Photolithography or optical lithography is a process used in semiconductor device fabrication to transfer a pattern from a photomask (also called reticle) to the surface of a substrate. Here, photolithography is just briefly described. Details can be found in various references, e.g. [2].

Photolithography involves a sequence of:

1. substrate preparation
2. photoresist application
3. soft-baking
4. exposure
5. reversal baking
6. flood exposure
7. developing

Substrate preparation

Prior the application of photoresist all residuals on the surface need to be removed by appropriate cleaning steps dependent on the substrate material. Special attention needs to be paid to moisture. Therefore silicon wafers are heated and coated with HDMS (hexa-methyldisilazane) which promotes a better adhesion between the photoresist and the wafer.

Photoresist application

The wafers are usually covered with photoresist by spin coating. Depending on the type of the resist and the functionality it should serve (dry etching, wet etching, long or short etching time etc.) the film thickness varies between 0.5 µm up to several micrometer. Typically AZ 5214E photoresist is spin coated at 4000 rpm to reach a film thickness of 1.4 µm followed by a soft bake at 90 °C for 5 minutes to drive off excess solvents.

Exposure

In general photoresists are classified into two groups, positive resists and negative resists.

- A positive resist is a type of photoresist in which the portion of the photoresist that is exposed to light become soluble to the photoresist developer and the portion of the photoresist that is unexposed remains insoluble to the photoresist developer.

- A negative resist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes relatively insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer.

Within the exposure the wafer with photoresist on top and the photomask are brought into contact by use of a so called “aligner”. The photomask is a quartz glass plate covered with structures, made from chromium. The structures need to be transferred to the wafer. This assemble is than irradiated with UV light, whereby in the non-covered parts the resist is exposed to the UV light. Note that for the cross-point structures the top electrode pattern has to be aligned to the bottom electrode pattern.

Image reversal

AZ® 5214 E is a special photoresist capable of image reversal. Exposed areas may be selectively cross-linked by a reversal bake at 120°C for 45 sec after the first exposure. A flood exposure of the full wafer converts formerly unexposed areas to soluble material, resulting in a negative tone image. The profile generated by such processing has a negative shape (wall profile) allowing for use in lift-off techniques (see Figure 5).

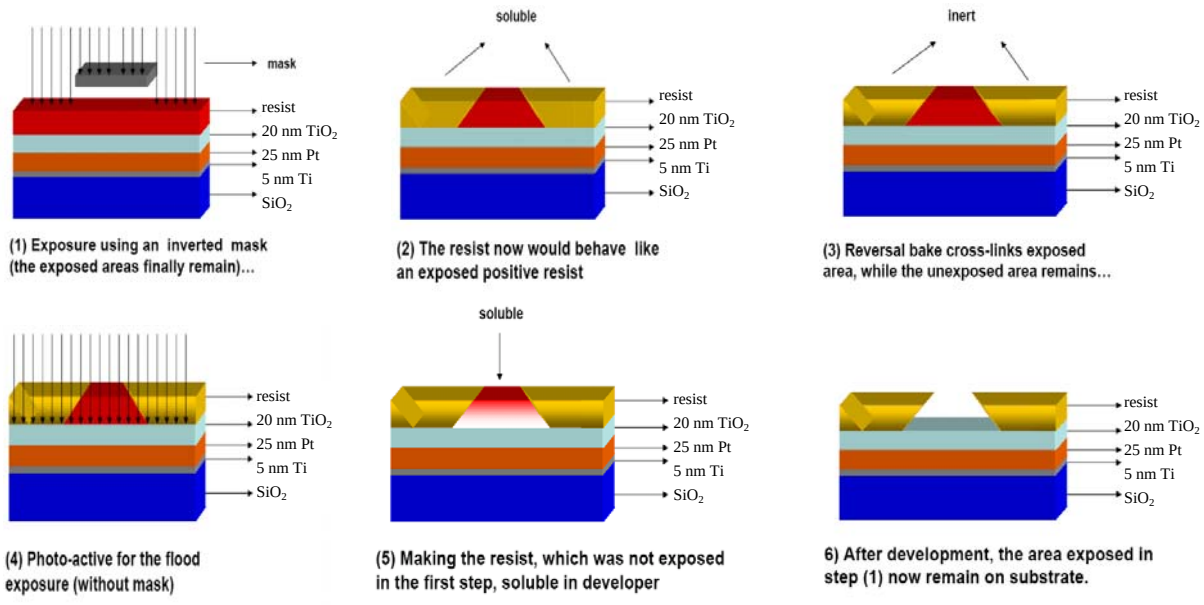


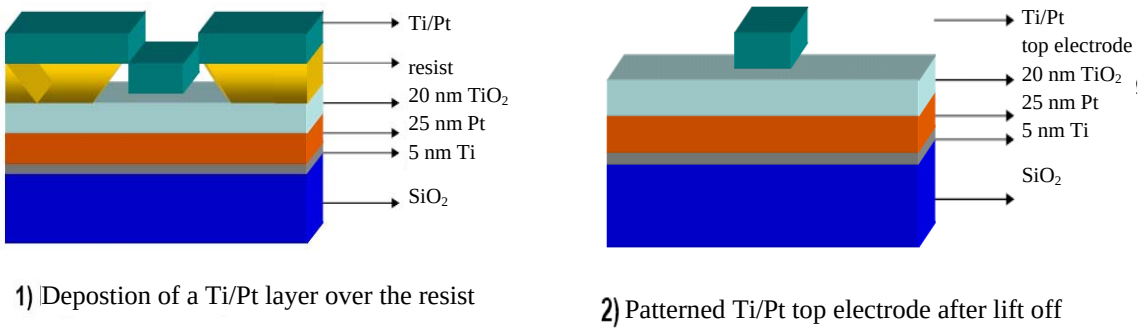
Figure 5: Photolithography - sequence of image reversal processing.

Developing

To release the soluble structures, the wafers are rinsed with in a developer. Developers often contain sodium hydroxide (NaOH). Also metal-ion-free developers such as tetramethylammonium hydroxide (TMAH) are used. By the use of a positive photoresist the developer removes all exposed areas, if a negative resist is used all areas which were unexposed in the first exposure step are removed.

Lift-off process

For preparation of the top electrode a Ti/Pt metal film will be sputtered over the whole chip area and patterned using the "Lift-off" process (Figure 6.1). During the lifting-off, the photoresist under the metal layer is removed with the solvent, taking the metal film on top with it, and leaving behind only the metal structures which were deposited directly on the TiO_2 layer (Figure 6.2).



1) Depostion of a Ti/Pt layer over the resist

2) Patterned Ti/Pt top electrode after lift off

Figure 6: Schematic of “lift-off” technique.

4) Sputter deposition of metal films

Sputtering belongs to the physical vapor deposition (PVD) techniques, as the thin film is deposited by condensation out of the vapor phase of the desired material. The sputtering system that will be used for the metal layer deposition is a Univex 450C from Leybold. This sputter machine is designed as a cluster tool with a load-lock and several chambers equipped with different materials like Pt or Ti, each connected to the transfer chamber. The setup enables a consecutive in situ deposition of different materials. For the fabrication of Pt and Ti thin films a DC-magnetron source will be used as depicted in Figure 7. This is adequate for

the pure metal targets, which are connected to the negative potential of the generator serving as cathode. The grounded substrate support establishes a high electrical field with the target. Pure Ar is injected into the chamber resulting in a working pressure between 5.1 and $13.5 \cdot 10^{-3}$ mbar. This pressure and the high electric field ignite an Ar^+ plasma, which is also termed glow discharge, due to its relatively low ionization degree. Under the given parameters and a DC input power of 375 W a deposition rate of 2.5 $Å \cdot s^{-1}$ for Pt can be achieved. A stack of 5nm Ti and 25 nm Pt will be deposited onto the sample with the structured resist pattern to obtain the final cross point electrode structure after accomplishing the 'lift-off' process (see Fig. 6).

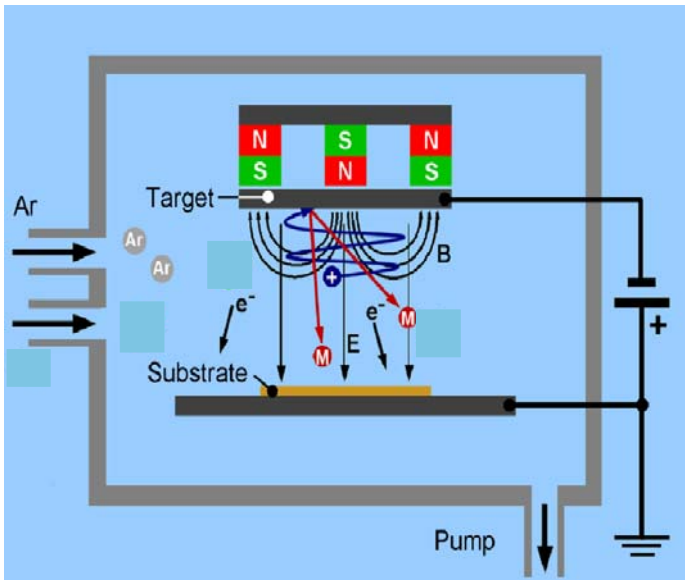


Figure 7: Schematic drawing of a dc-magnetron sputtering process. [5]

5) Measurement of test devices

Besides the surface- and structural analysis with SEM, XRD, AFM etc. (not part of this course, more information can be found in [3]), the electrical characterization is one major part to investigate the material properties in order to realize materials for resistive RAM.

The typical test sample is shown in Figure 1, where the functional film (e.g. TiO_2) is sandwiched between the lines of bottom and top electrodes of different width. The active area during the electrical measurements is thereby reduced to the area of the cross junction. Since the lateral size of the contact point is a factor of 100 to 1000 larger than the film thickness (typically 10-20 nm) one may neglect fringe effects.

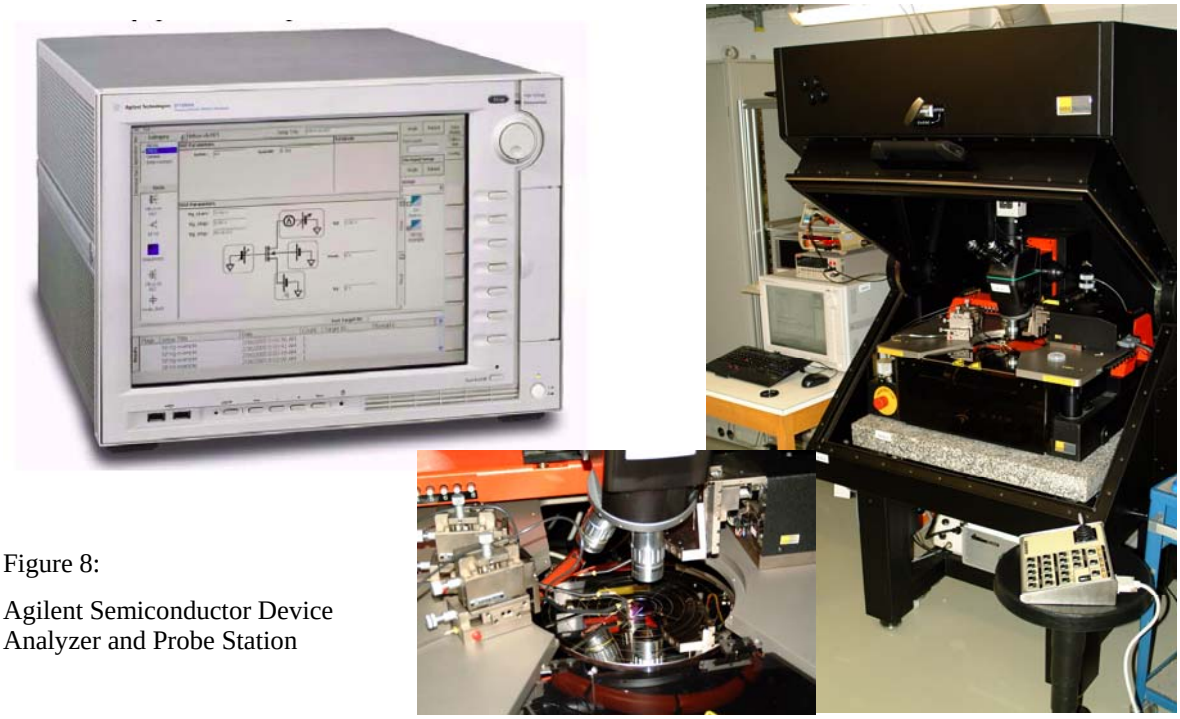
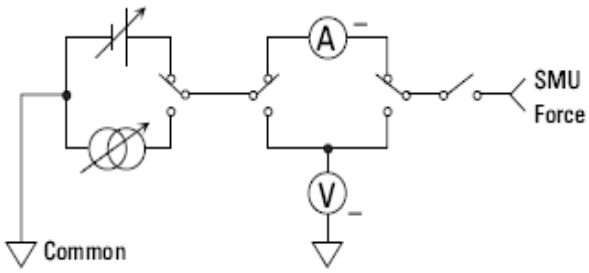


Figure 8:

Agilent Semiconductor Device Analyzer and Probe Station

The electrical testing is performed using a Semiconductor Device Analyzer in combination with a Probe Station in order to achieve good connection and sufficient shielding against interferences from the environment (Fig. 8). The Agilent B1500A provides the DC voltage/current output capability, the DC voltage/current measurement capability, and the AC signal output and impedance measurement capability. So you can perform the current-voltage sweep measurement and the capacitance voltage sweep measurement for example by one instrument.

Since the novel memory type relies on the fact that each cell can have two different resistance states, indicating the digital “0” and “1”, and the change between those different states is performed by exceeding a threshold voltage, the most important measurements are I(V)-characteristics. The analyzer provides four so called source/monitor units (SMU), which can apply DC voltage or current, and can measure DC current or voltage. Figure 9 shows a simplified SMU circuit diagram. The SMU can perform the following operations:



- Apply voltage and measure current
- Apply current and measure voltage
- Apply voltage and measure voltage
- Apply current and measure current

Figure 9: Simplified SMU Circuit Diagram [4].

The SMU has a compliance feature that limits output voltage or current to prevent damage to the device under test. When the SMU applies voltage, you can specify the current compliance. When the SMU applies current, you can specify the voltage compliance.

The characteristic parameters of a typical current vs. voltage I(V) measurement are shown in Figure 10. A measurement begins with setting the electrical potential to a start value and holding it for a certain time in order to decay relaxation effects and to get stable measurement condition. Then the voltage is increased stepwise and after a delay time (t_{delay}) the current is measured during the integration time ($t_{integrate}$). This procedure is repeated until the stop value is reached (single sweep) or the stop value is reached and the voltage is decreased again until the starting voltage (double sweep). All parameters like hold time, delay time, start and stop potential, step height, number of steps etc. are free programmable and depend strongly on the sample material and type of conducting mechanism.

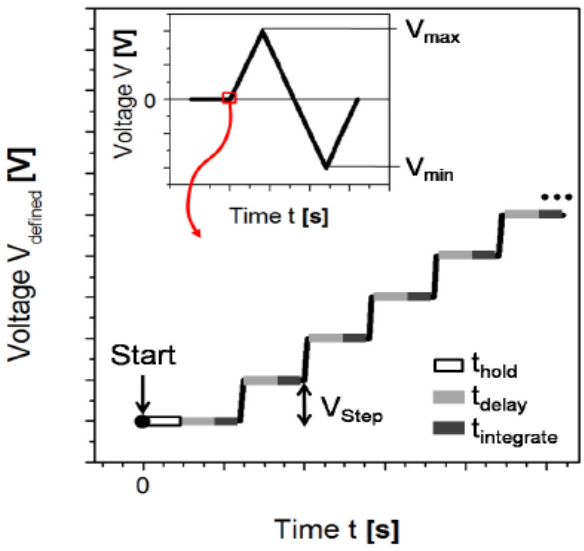


Figure 10: Characteristic parameters of a voltage sweep measurement [4], [5].

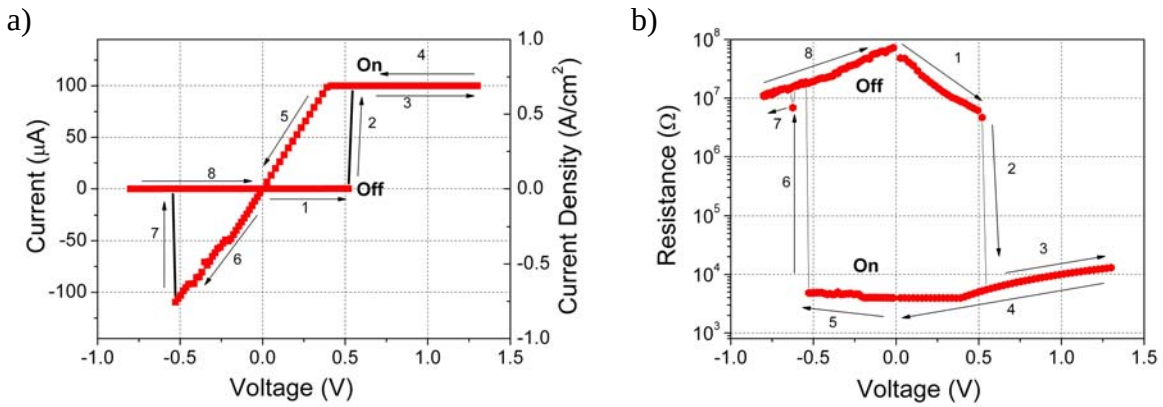


Figure 11: a) current – voltage characteristic: I(V) and b) resistance – voltage characteristic: R(V) of a TiO_2 thin film sample.

Some typical measurement results are presented in Figure 11a, b. Initially the sample is in "off" state corresponding to a low current (Fig. 11a) and high resistance (Fig. 11b). By exceeding a threshold voltage of +0.5 V the resistance decreases dramatically and the current is limited to the current compliance of 100 µA. Decreasing the voltage results in a hysteretic behaviour (arrow 5) indicating a higher current and a low resistance. Reversing the potential leads to an abrupt decrease of the current when exceeding -0.5 V, which means that the sample switches back from the low resistance state (LRS) to the high resistance state (HRS) corresponding to the change from "1" to "0". Since the different states are stable without any applied voltage this memory technology is non-volatile.

References

[1] "Atomic Layer Deposition" by M. Ritala, M. Leskelä, in Handbook of Thin Film Materials - Vol. 1, ed. H.S. Nalwa, Academic Press, (2002).

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