JÜLICH Forschungszentrum | JÜLICH SUPERCOMPUTING CENTRE

Full Availability of JURECA-DC Module

The JURECA-DC module – DC for data-centric – is a supercomputer with innovative support for data-intensive applications. Its first phase with 384 CPU nodes, each with 128 AMD EPYC Rome cores per node, and 48 nodes additionally equipped with four NVIDIA A100 GPUs, entered production in December 2020 as the successor of the JURECA Cluster module.

On 1 May 2021, the second phase of the JURECA-DC module was brought online – right in time for the start of the new computing-time period. The system now consists of 480 CPU nodes of the aforementioned CPU type with 512 GB memory each, 96 CPU nodes with 1024 GB memory each, as well as 192 GPU nodes with 512 GB of memory and four A100 GPUs each. The compute nodes and login servers are interconnected by a Mellanox InfiniBand HDR network. User access is possible through 12 login servers.

The theoretical peak performance is now 18.52 petaflops, with 14.98 petaflops on the GPUs and 3.54 petaflops on the CPUs. In its final configuration, the JURECA-DC module has 8 times the performance of its predecessor, the JURECA Cluster module.

Within the JURECA-DC module, additional features are available, like a cluster-local network-accessible NVMe-based storage system, additional profiling capabilities, and an energy optimizer. Further information on JURECA-DC, its configuration, and the available tools can be found at https://fz-juelich.de/ias/jsc/jureca.

The JURECA-DC module was procured as part of the EU-funded PPI4HPC project, in which computing centres from four European countries have united to purchase new, innovative supercomputer systems through a joint procedure – for the first time at the European level. A share of its resources will therefore be available to European researchers. Predominantly, computing time on JURECA-DC will be granted to researchers at Helmholtz centres, and in particular to researchers at Forschungszentrum Jülich.

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Arm and Forschungszentrum Jülich Sign Multi-Year Collaboration Agreement

The microprocessor company Arm and Forschungszentrum Jülich have signed a multi-year collaboration agreement to strengthen their joint efforts in identifying the requirements of high-performance computing (HPC) applications and advancing their porting and optimization on Arm-based architectures. Chips with Arm architecture are found in virtually all smartphones and the vast majority of tablet computers. In addition, Arm processors are also increasingly used in supercomputers, for example in the Japanese supercomputer Fugaku, which is currently the fastest computer in the world. The Arm design is also the basis for the development of the first European HPC processors within the European Processor Initiative (EPI project), in which JSC is participating.

The collaboration between Arm and JSC focuses on the analysis and optimization of strategic HPC applications on Arm-based HPC systems, including Arm-accelerated platforms (for example, Arm+GPU). The joint team carries out performance analyses and code engineering, taking advantage of specific features of Arm-based hardware to further advance application performance. The code requirements identified in this effort will contribute to the design of future HPC technologies and systems. More information, including a video message by Brent Gorda from Arm and Thomas Lippert from JSC, can be found at https://fz-juelich.de/ias/jsc/arm-collaboration.

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JSC@ISC2021

The conference ISC High Performance 2021 Digital will take place from 24 June to 2 July 2021 as an online event (https://www.isc-hpc.com/).

JSC, together with its partners in the Gauss Centre for Supercomputing (GCS) – HLRS in Stuttgart, and LRZ in Garching – will present its wide-ranging supercomputing activities at the virtual GCS booth (https://isc.gauss-centre.eu). Focus topics are the path to exascale with JSC's modular supercomputing architecture (MSA)

concept, the steadily increasing importance of AI in HPC reflected, e.g. by the Helmholtz AI Cooperation Unit, and quantum computing technologies, where the growing Jülich UNified Infrastructure for Quantum computing (JUNIQ) will be presented.

JSC employees will furthermore contribute to the event with numerous talks and workshops. Some examples include: Martin Schultz's invited talk entitled "Is bigger always better? Deep learning applications in air quality research"; Bernd Mohr's "Introduction to HPC: Applications, Systems, and Programming Models"; and Christian Witzler's talk in the "5th Workshop on In Situ Visualization" on "Including in situ visualization and analysis in PDI". Christian Feld, Markus Geimer, and Brian Wylie are co-organizing the tutorial "Hands-on Practical Hybrid Parallel Application Performance Engineering" and Alan O'Cais will speak about "Maintaining a Modern Scientific Software Stack Made Easy with EasyBuild". Furthermore, there will be a one-to-one conversation between Kristel Michielsen (JSC) and Matthias Troyer (Microsoft) on 1 July.

Detailed information on JSC's participation and activities can be found at https://fz-juelich.de/ias/jsc/isc21.

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News from the NIC Scientific Council

The Scientific Council of the John von Neumann Institute for Computing (NIC) held its annual meeting on 22 April 2021. The meeting was conducted by chairman of the council Prof. Marcus Müller (University of Göttingen). Prof. Christine Peter (University of Konstanz) took up her duties as deputy chairwoman of the NIC Scientific Council. Dr. Joanna Staneva (Helmholtz-Zentrum Hereon) was elected new member and will begin her term in January 2022. The term of office for Prof. Daniela Jacob (Climate Service Center, Hamburg) ends on 31 December 2021. Prof. Müller expressed his thanks to Prof. Jacob for her previous work on the NIC Scientific Council.

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New GCS Large-Scale Projects Started in May 2021

Twice a year, the Gauss Centre for Supercomputing (GCS) issues a call for large-scale projects on its petascale supercomputers – Hawk (HLRS), JUWELS (JSC), and SuperMUC-NG (LRZ). Projects are classified as large-scale if they require at least 2 % of the systems' annual production in terms of estimated availability.

After computing time quantities were previously specified in core hours, the modularity of JUWELS requires the introduction of a new computing time unit. JSC is currently working with the peak floating point operations per year (FLOP/a) of the computing devices (CPU or GPU) available to approved projects. The computing time on Hawk and SuperMUC-NG continues to be given in core hours. Projects in this case fall into the category of large-scale only if they require at least 100 Mcore-h on Hawk, or 45×10^{21} FLOP/a on JUWELS, or 45 Mcore-h on SuperMUC-NG.

The GCS Peer Review Board decided to award the status of a large-scale project to 14 projects from various scientific fields. Two of these projects requested computing time on two of the three available systems. In total, three projects were granted 950 Mcore-h on Hawk, another four projects were granted 227×10^{21} FLOP/a on JUWELS, and nine projects were granted 654 Mcore-h on SuperMUC-NG.

For more details on these projects, visit https://www.gauss-centre.eu/results/large-scale-projects/.

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JSC Companion Prof. Josef Dietrich Haupt Passed Away

With deep regret, JSC is sad to announce that on 13 May 2021, its long-time companion Josef Dietrich (Dieter) Haupt, Professor Emeritus at RWTH Aachen University, passed away. He was one of the directors at the RWTH computer centre in the 1980s and 1990s. Beyond RWTH, he was significantly involved in the expansion and shaping of the science system in Germany – including co-founding the DFN-Verein and the Gesellschaft für Informatik. JSC will remember him above all as a founding member of the Scientific Council of the then "Höchstleistungsrechen-zentrum" (High-Performance Computing Centre) at Forschungszentrum Jülich. In this role, he accompanied and strengthened the development of high-performance computing in Jülich until the foundation of the John von Neumann Institute (NIC). Colleagues at NIC will remember him fondly.

Events

Introduction to parallel programming with MPI and OpenMP
Instructors: Benedikt Steinbusch, Thomas Breuer, JSC
Date: 9–13 August 2021, 09:00–16:30
Venue: online
https://fz-juelich.de/ias/jsc/2021/mpi-intro-2

For further events, talks, and training courses see,
https://fz-juelich.de/ias/jsc/events