# JURECA

## General-Purpose Supercomputer

### Jülich Research on Exascale Cluster Architectures

- Combining versatile multi-core Cluster with highly-scalable many-core Booster
- Implements architecture devised in DEEP and DEEP-ER projects in production system
- Applications can be mapped to individual modules or distributed across both
- Research vehicle for next-generation cluster architectures
- Project partners: T-Platforms, Intel, Dell, ParTec

### System architecture

- Multi-core processor based Cluster module: 2.2 Petaflop/s peak performance in 34 racks
  - 45,216 Intel Haswell cores, 272 TiB main memory
  - 100 Gb/s Mellanox EDR interconnect with non-blocking full fat tree topology
- Many-core processor based Booster module: 5 Petaflop/s peak performance in 33 racks
  - 111,520 Intel Knights Landing cores, 154 TiB main memory
  - 100 Gb/s Intel Omni-Path interconnect with non-blocking full fat tree topology
- 20 Tb/s cross-module communication bandwidth

### Software

- Unified software stack for Cluster and Booster modules
- CentOS 7 Enterprise-Linux distribution
- ParaStation Global MPI
- Slurm batch system with ParaStation resource management


*JURECA Cluster module*

*JURECA Booster module*

**Contact:** p.thoernig@fz-juelich.de, d.krause@fz-juelich.de | **Website:** www.fz-juelich.de/ias/jsc/jureca