JÜLICH Forschungszentrum | JÜLICH SUPERCOMPUTING CENTRE

QUANTUM INFORMATION PROCESSING

SIMULATION ON/OF QUANTUM COMPUTERS

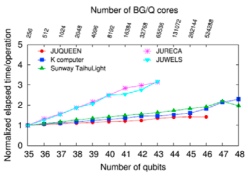
- **High performance computing for simulating the real-time dynamics of quantum computers up to 48 qubits**
- **Simulation of physical models of multi-qubit systems**
- **Exploration of support vector machines on the D-Wave quantum annealer**
- **Exploration and performance tests of the IBM Quantum Experience with 5 and 16 qubits and of the CAS-Alibaba quantum processor with 11 qubits**

Ideal quantum computer

Massively parallel quantum spin dynamics simulator simulates N ≥ 40 qubit quantum computer on JURECA, JUQUEEN, JUWELS, K and Sunway TaihuLight

- Simulator to develop and test quantum algorithms and applications
- Beats exponential scaling: wall clock time O(N)

H. De Raedt, et al., Massively parallel quantum computer simulator, eleven years later, Comp. Phys. Comm. 237, 47-61 (2019)



Weak scaling behavior for executing a CNOT operation on each subsequent pair of qubits. The elapsed time is normalized by the values for the 35-qubit circuit

- Used to benchmark Sycamore, Google's 53-qubit quantum processor which achieved quantum supremacy

F. Arute, et al., Quantum supremacy using a programmable superconducting processor, Nature 574, 505-510 (2019)

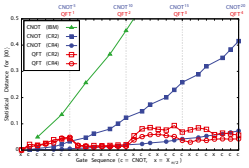
Superconducting qubits

Simulation of the real-time dynamics of a system of

- two superconducting flux qubits (rf-SQUIDS) coupled by an rf-SQUID, the building blocks of the D-Wave quantum processors, shows that the system can be well described by two spin-1/2 qubits coupled by an harmonic oscillator

M. Willsch, et al., Real-time simulation of flux qubits used for quantum annealing, arXiv:1906.07024

- two transmon qubits coupled by a resonator, the building blocks of the 5-qubit IBM QX device, shows that the system modelled as the lowest eigenstates of two Cooper Pair Boxes in the transmon regime coupled to an harmonic oscillator cannot be represented by two spin-1/2 qubits coupled to an harmonic oscillator



On a transmon qubit device a CNOT gate can be implemented as a two-pulse (four-pulse) echoed cross-resonance gate CR2 (CR4). One Quantum Fourier Transform (QFT) consists of 5 CNOT gates and two $X_{\pi/2}$ gates.

Simulation and IBM QX results show that gate metrics provide insights into errors of the implemented gate pulses, but this information is not enough to assess the error induced by repeatedly using the gate in quantum algorithms.

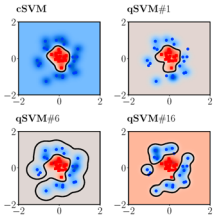
D. Willsch et al., Gate error analysis in simulations of quantum computers with transmon qubits, Phys. Rev. A 96, 062302 (2017)

D-Wave quantum annealer

Binary classification by Support Vector Machines (SVM), a supervised machine learning algorithm:

- Classical SVM (cSVM): training corresponds to a convex quadratic optimization problem, one of the rare minimization problems in machine learning having a global minimum. The global minimum for the training dataset is not necessarily optimal for the test dataset
- Quantum SVM (qSVM) on a D-Wave quantum annealer: quantum annealer produces various close-to-optimal solutions for the training data, whereby the different solutions often emphasize different features of the training data. Combination of these solutions to test data might solve the classification task better than cSVM.

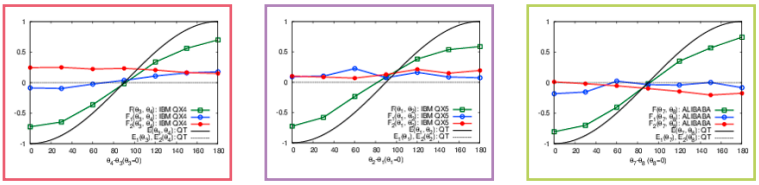
D. Willsch, et al., Support vector machines on the D-Wave quantum annealer, Comp. Phys. Comm. (in press)



Classification boundary resulting from the global optimum produced by cSVM, and from the ensemble produced by qSVM.

IBM Quantum Experience (IBM QX) and CAS-Alibaba

Performance test of the IBM QX4 (5 qubits), IBM QX5 (16 qubits) and CAS-Alibaba (11 qubits) quantum processors by means of measurement of the singlet state.



Data for a quantum-gate circuit which, theoretically, generates the singlet state. Black lines: results from quantum theory; colored symbols: results from measurements on the quantum devices; colored lines: guides to the eye.

- The results only qualitatively agree with quantum theory.
- Deviations are not within 5 standard deviations.

K. Michielsen et al., Benchmarking gate-based quantum computers, Comp. Phys. Comm. 220, 44 (2017)

K. Michielsen, et al Simulation on and HPC simulation of quantum computers and annealers, in Future Trends of HPC in a Disruptive Scenario, eds. Grandinetti, L., Joubert, G.R., Michielsen, K., Mirtaheri, S.L., Taufer, M., Yokota, R., Volume 34 of Advances in Parallel Computing (IOS Press, Amsterdam, 2019)

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